sPHENIX Silicon Tracker R&D

Y. Akiba (RIKEN/RBRC)

2015/11/09

sPHENIX Cost and Schedule Review

Proposed Si Tracker

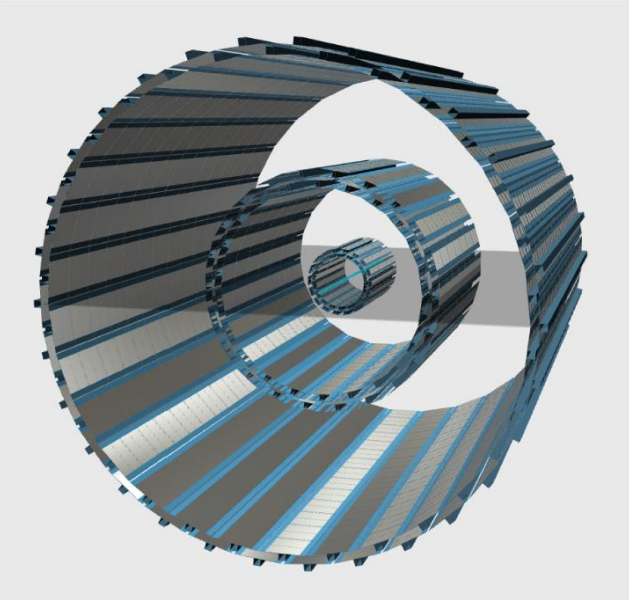


Figure 4.1: CAD drawing of the silicon strip tracker.

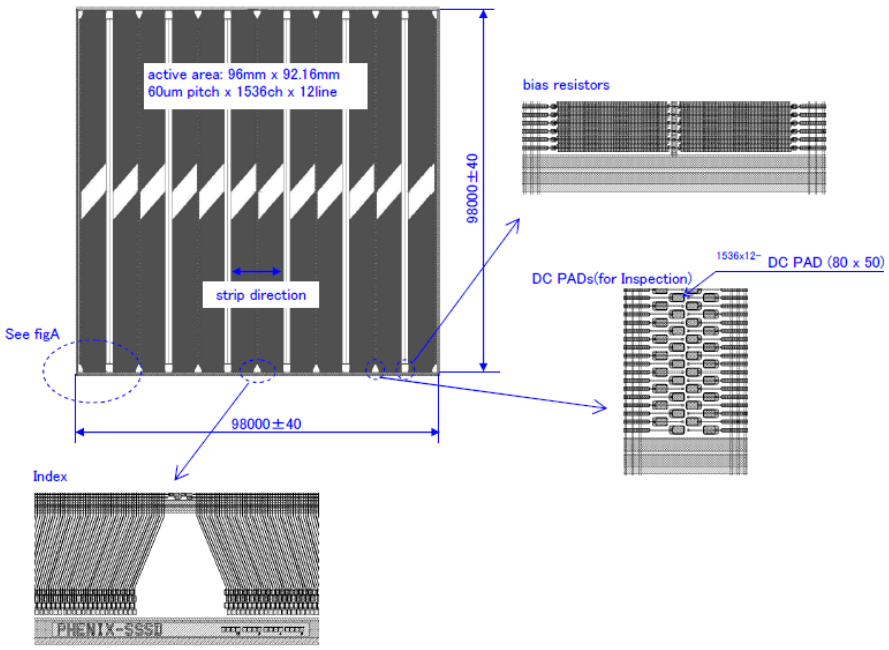
Station	Layer	radius (cm)	pitch (μm)	sensor length (cm)	depth (μm)	total thickness X_0%	area (m^2)
Pixel	1	2.4	50	0.425	200	1.3	0.034
Pixel	2	4.4	50	0.425	200	1.3	0.059
S0a	3	7.5	58	9.6	240	1.0	0.18
S0b	4	8.5	58	9.6	240	1.0	0.18
S1a	5	31.0	58	9.6	240	0.6	1.4
S1b	6	34.0	58	9.6	240	0.6	1.4
S2	7	64.0	60	9.6	320	1.0	6.5

Table 4.3: Number of channel summary for the silicon strip tracker.

station	sub-layer	silicon modules per ladder	# of ladders	# of sensors
s0	2	3	36	216
s1	2	7	44	616
s2	1	14	48	672

- FPHX chip for read-out.
  - 128ch/chip. 3bit ADC /ch.
  - Low power (64mw per chip)
- Air cooling to achieve small radiation length
  - Separate 3 Upsilon states in small over-all size
- S0+S1+S2: ~10m^2 of silicon and 3.1 M ch

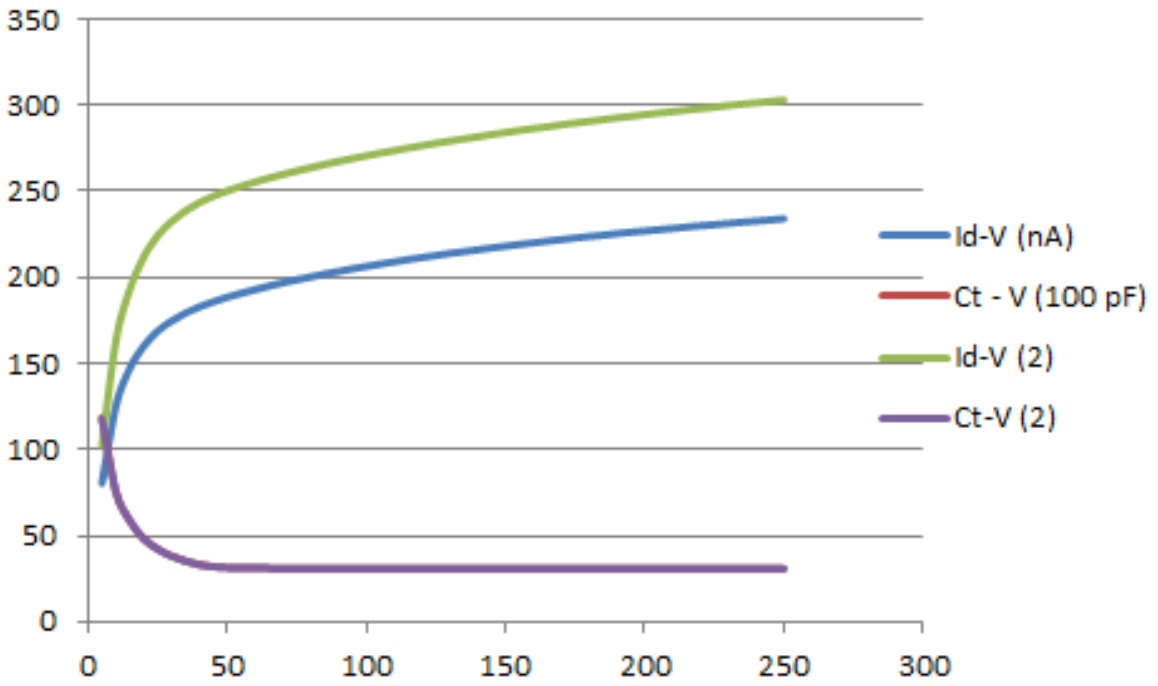
Silicon tracker R&D at RIKEN (JFY2014)



- Silicon sensor R&D at RIKEN in JFY2014
- Large Prototype sensor for the outer most layer
  - 96 mm x 92.16mm active area
  - 320 μm thick
  - AC coupled
  - 6x128x24 mini-trips (60μm x 8mm)
  - 128x24 read-out channels
- 5 sensors manufactured at Hamamatsu and delivered to RIKEN in March 2015
- For all of 5 delivered sensors
  - No NG channels or strip
  - Vfd = 50 V
  - Vbreakdown > 250V (>500V for two)
- All 5 sensors are now at BNL for testing

I-V, C-V data of prototype sensor

Serial. No. / Vr	1		2	
	Id [nA]	Ct [pF]	Id [nA]	Ct [pF]
5 V	80.4	11878.3	102.7	11774.7
10 V	125.4	7549.6	163.2	7530.3
15 V	147.0	5871.2	192.9	5878.8
20 V	160.2	4822.0	211.9	4813.4
25 V	168.8	4226.2	224.3	4216.4
30 V	174.7	3819.8	232.5	3810.9
35 V	179.3	3523.5	238.7	3515.9
40 V	182.9	3316.4	243.5	3310.3
45 V	185.9	3195.9	247.2	3191.6
50 V	188.5	3147.9	250.3	3143.8
55 V	190.8	3127.2	253.0	3122.5
60 V	192.9	3115.9	255.5	3111.6
65 V	195.0	3107.7	257.8	3103.8
70 V	196.9	3103.0	259.9	3099.7
75 V	198.7	3099.6	261.9	3096.5
80 V	200.3	3097.5	263.8	3093.6
85 V	202.0	3095.4	265.7	3091.2
90 V	203.5	3093.7	267.4	3088.8
95 V	205.0	3091.8	269.1	3088.5
100 V	206.4	3090.7	270.7	3086.9
105 V	207.8	3089.7	272.3	3085.6
110 V	209.1	3088.1	273.7	3084.6
115 V	210.4	3087.1	275.2	3083.9
120 V	211.6	3086.9	276.6	3082.7
125 V	212.8	3085.5	278.0	3081.9
130 V	214.0	3084.9	279.3	3080.8
135 V	215.0	3084.3	280.5	3080.8
140 V	216.1	3083.3	281.8	3079.7
145 V	217.2	3082.8	283.0	3079.5
150 V	218.2	3082.4	284.2	3078.8
155 V	219.2	3082.2	285.4	3078.4
160 V	220.1	3081.4	286.5	3077.8
165 V	221.1	3081.0	287.5	3076.8
170 V	222.0	3080.3	288.7	3077.1
175 V	222.9	3080.1	289.7	3076.3
180 V	223.8	3079.9	290.7	3076.3
185 V	224.6	3079.3	291.7	3075.6
190 V	225.5	3078.7	292.7	3075.2
195 V	226.3	3079.4	293.6	3074.8
200 V	227.0	3078.4	294.6	3073.8
205 V	227.8	3078.3	295.5	3074.1
210 V	228.5	3077.9	296.4	3073.8
215 V	229.3	3077.1	297.3	3073.5
220 V	230.0	3077.0	298.1	3072.6
225 V	230.7	3076.8	298.9	3073.0
230 V	231.4	3076.5	299.9	3072.5
235 V	232.1	3076.4	300.7	3072.1
240 V	232.8	3075.9	301.5	3072.1
245 V	233.4	3075.9	302.3	3071.4
250 V	234.1	3075.4	303.1	3071.6
Vfd [V]	50		50	
NG Strip	Nothing		Nothing	

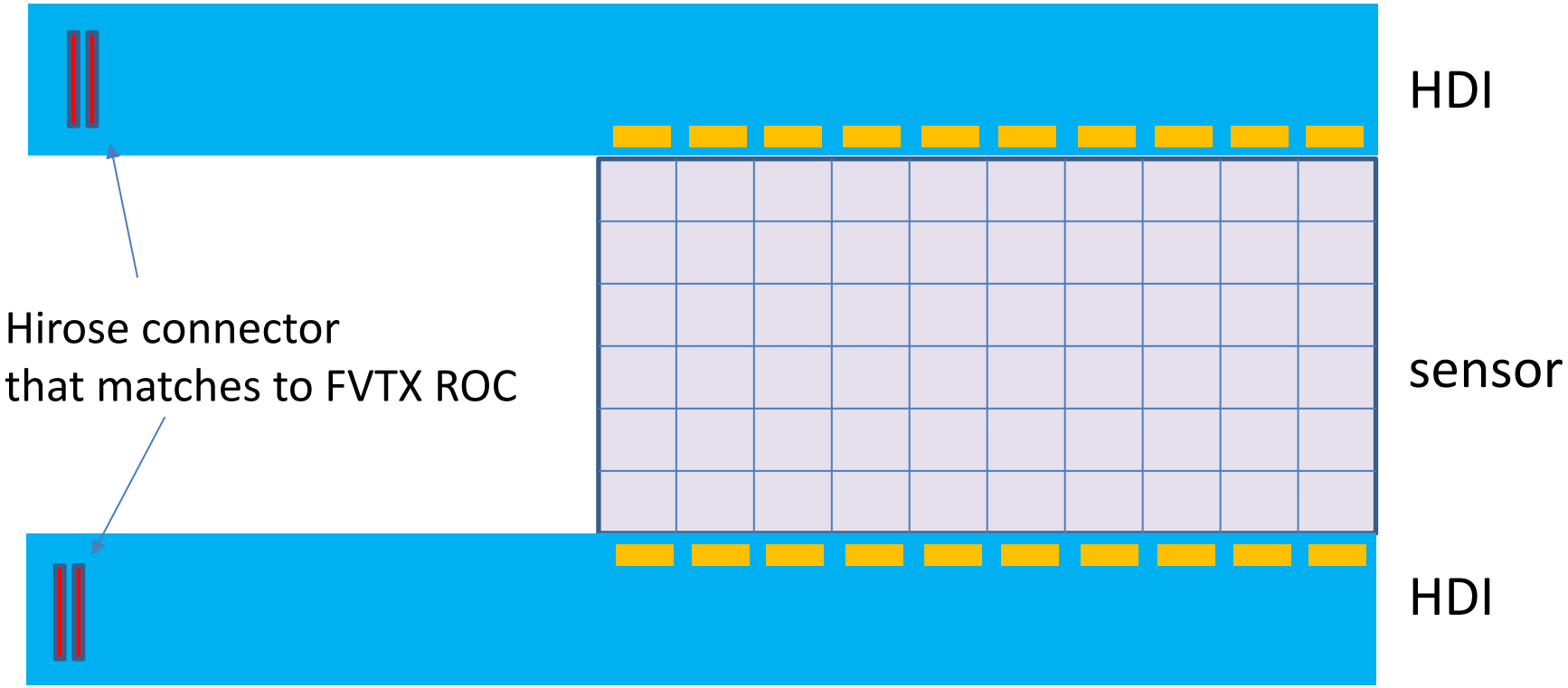


- Vfd: 50V
- No NG channels
- Breakdown V > 250V

R&D at RIKEN in JFY2015

- Plan:
  - Develop prototype S1 sensor (~5cm x 10cm, 2 sensors per wafer) at Hamamatsu
    - 320 um sensor and 240 um sensor will be made
  - Develop HDI (read-out FPC)
  - Assemble them into prototype Silicon Modules
  - Test and evaluate the silicon module using FVTX test bench
    - The module will be made to be electrically same as “small wedge” of FVTX
- Goal:
  - Test S1 Silicon Module by March 2016

Conceptual design of S1 Sensor Module prototype



- HDI width: ~20 mm
- HDI length: ~40 cm including the bus part
- Radiation length: 0.28% (physical thickness 0.45mm)
- Electrically the same as the small Wedge HDI of FVTX. This allows read-out via FVTX ROC+FEM

S1 Sensor Prototype

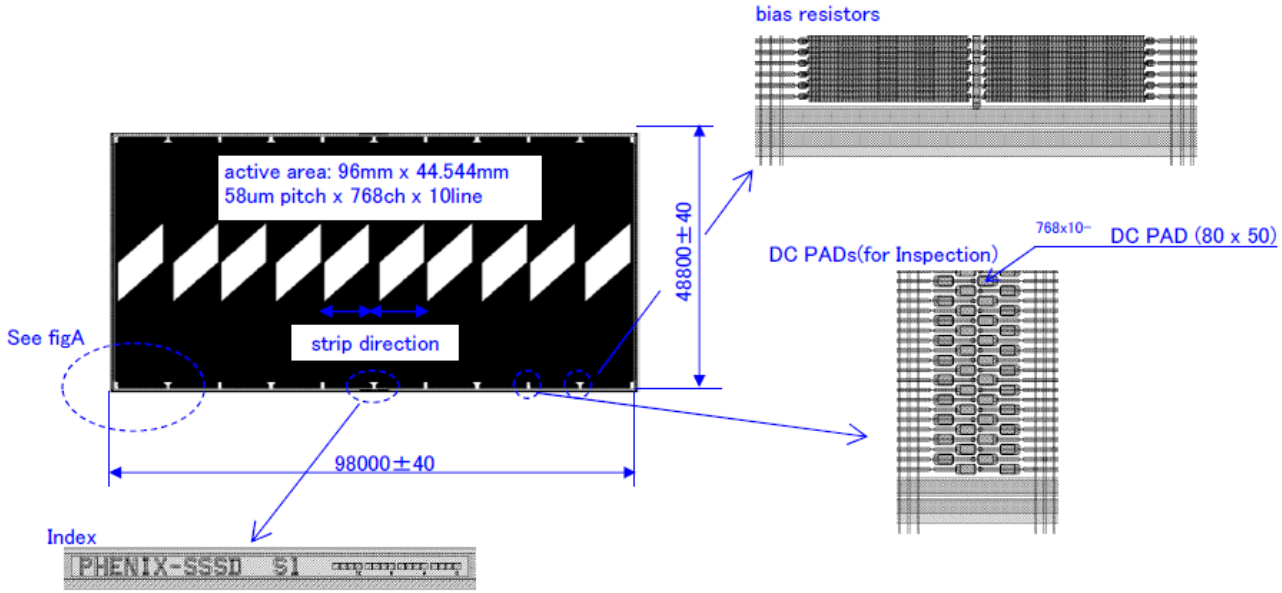
Plan:

- Make sensors with two thickness
  - 320 um thick 4 sensors
  - 240 um thick 4 sensors
- Two types of sensors are the same except for the thickness.
  - 320 um sensors are made by the HPK standard process.
  - 240 um sensors are made by thinning of the backside of 320 um sensors
- Expected ENC is about 1000. So the 320 um sensor is expected to have S/N~20 and the 240 um to have S/N~15.
- All sensors will be tested by HPK (IV/CV curves, test of all channels and strips) and only good sensors will be delivered.

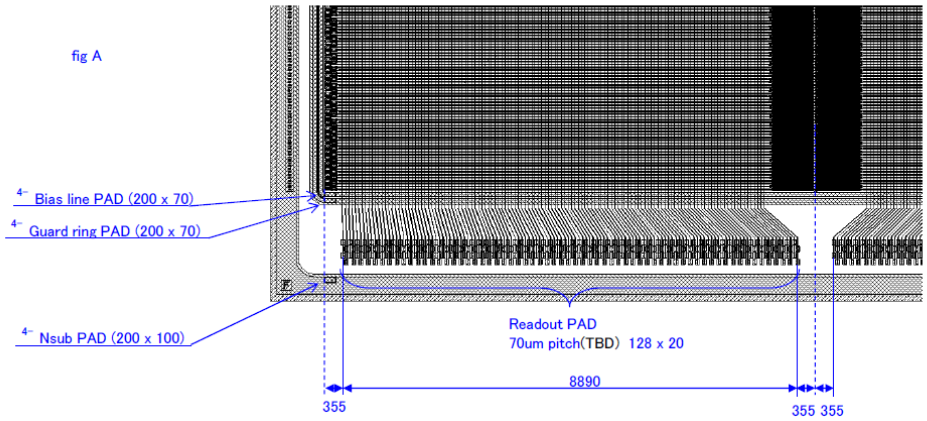
Status:

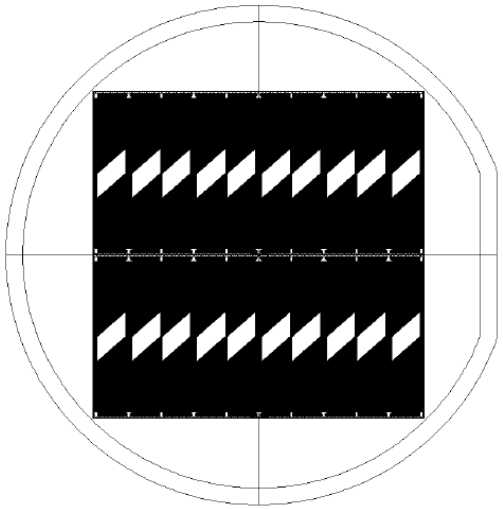
- The contract was made on 8/26
  - Delivery of the 320 um by December 1st
  - Delivery of the 240 um sensors in the middle of January

HPK design of S1 sensor



wafer layout S1





2chip/wafer

Received from HPK (2015/06/16)

HDI

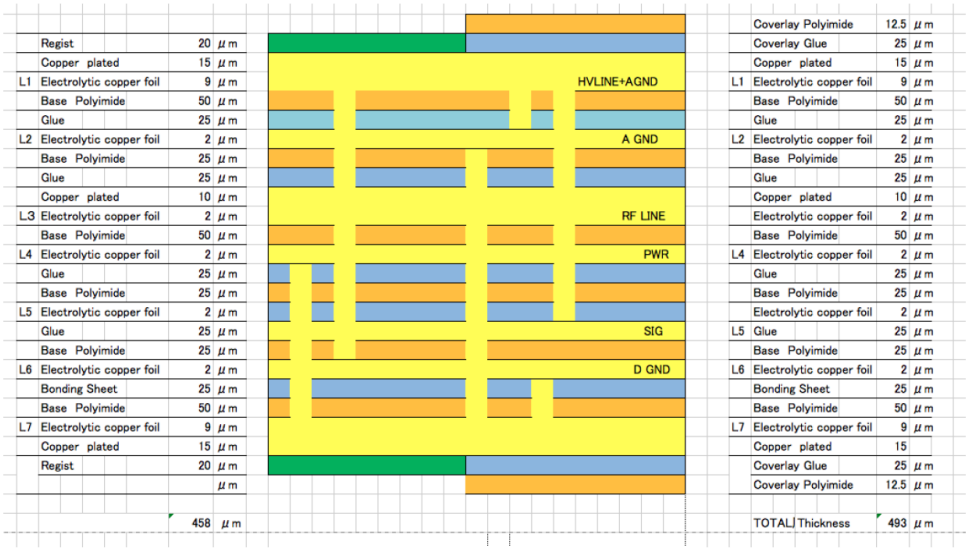


Figure 4.17: The 8 layers structure of the HDI for S1 layer.

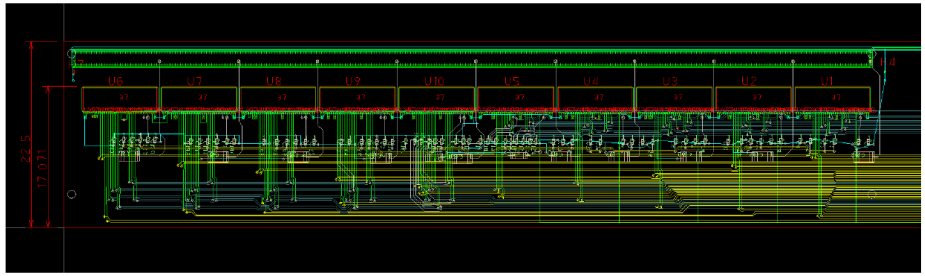
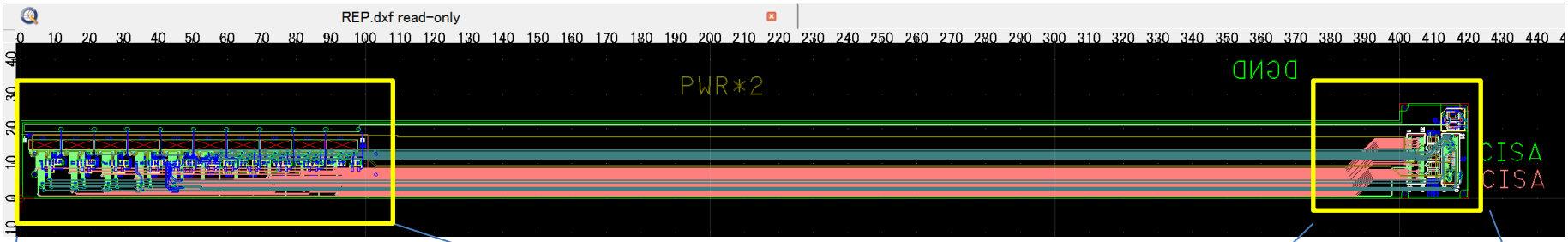


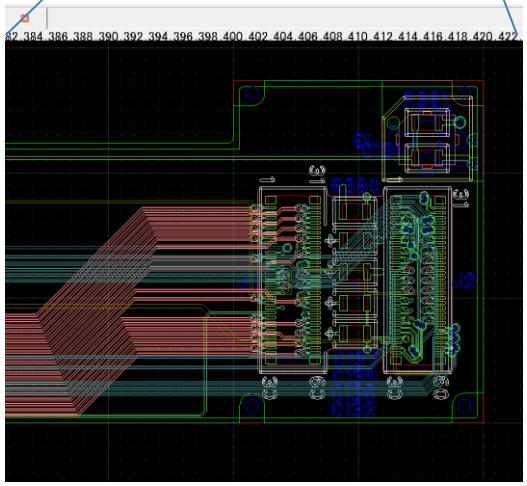
Figure 4.18: The circuit drawing of HDI for S1 layer drawn by Inoue Meterial Co.

- HDI (FPC to read-out the sensor) design is in progress at Yamashita Co. in Tokyo
- Layer structure follows that of FVTX HDI
- Received the design file on 10/21

HDI design



Total length: ~ 420 mm
Width: ~20mm



- Checking the Layout now
- Fabrication of 10 pairs will start soon

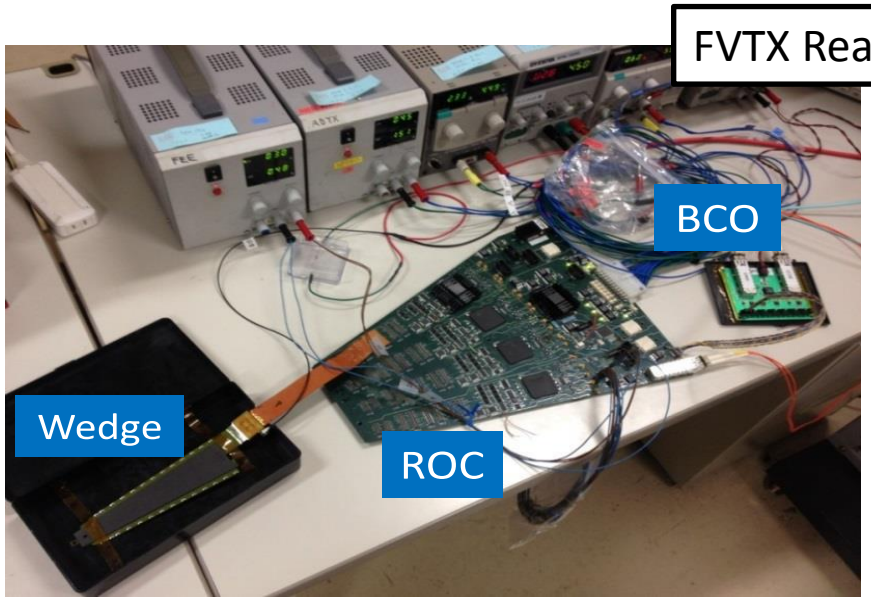
FPHX chips

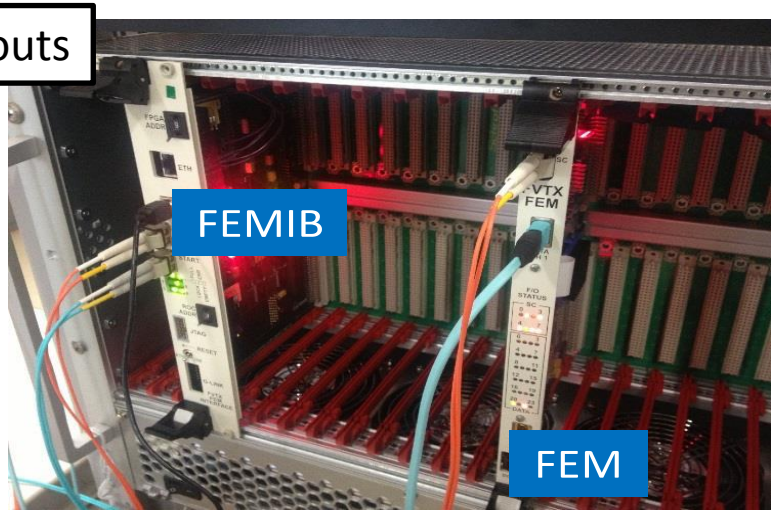
- There are 8 undiced wafers (1 probed, 7 un-probed) left from FPHX production for FVTX
- In FVTX production, the yield of good chip is high (>98%)
- 1 probed wafers diced and about 600 diced chips are now at BNL
  - These diced FPHX chips will be used for the S1 Silicon module prototype
- 2 or 3 more wafers will be sufficient for the R and D stage.
- For the full Si-Tracker, we need a new production of FPHX.
  - The masks used in the FVTX production is still available.

Plan for Silicon module assembly

- The present plan is to assemble modules at BNL
  - Prototypes of VTX stripixel silicon modules were assembled/wire bonded at BNL
- We will first put FPHX chips on HDI, and test and debug the HDI without sensor using FVTX test bench at BNL
- After the test, a sensor and two HDIs will be wire-bonded to make a silicon module
- We will make modules of 320 um thick sensor first, and then will make modules of 240 um thick sensor

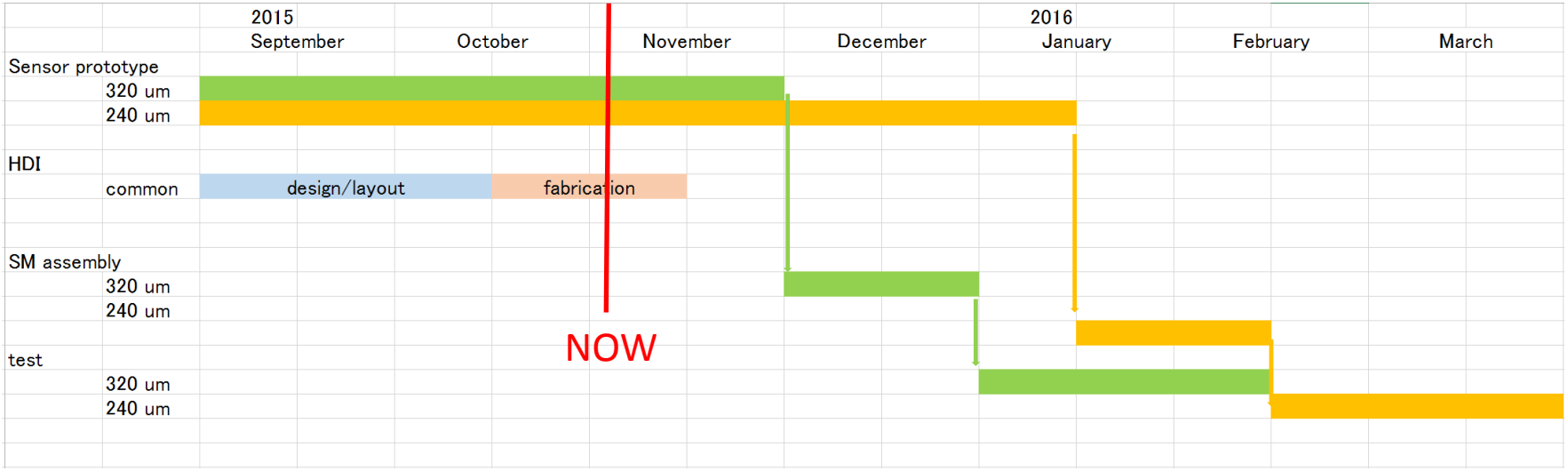
Silicon module test





- HDI of the S1 silicon module is Electrically same design as the “small wedge” of FVTX
- Assembled S1 modules will be tested at BNL and LANL to evaluate
  - S/N of MIP signal for single module (S/N~15 expected for 240 um sensor)
  - Data read-out speed
  - Cross talks between multiple modules on the same ladder
  - Etc
- If 240 um sensor shows good S/N, we ill chose this as the thickness of S1 layer. Depending on S/N, we will try even thinner sensor in the next round.

Time line of R and D



- The schedule above was made in August. We are basically on schedule
- Both types of SMs (320um sensor, 240um sensor) will be tested by the end of JFY (Mar 2016)
- In JFY2016, we will continue the R&D to make a full ladder prototype of S0, S1 and S2.